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Patentanmeldung Nr. **Patent application No.** **Demande de brevet n°**

02368113.3

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
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Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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International Business Machines Corporation
Armonk, N.Y. 10504
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Coaxial via structure for optimizing signal transmission in multiple layer electronic device carriers

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COAXIAL VIA STRUCTURE FOR OPTIMIZING SIGNAL TRANSMISSION IN MULTIPLE LAYER ELECTRONIC DEVICE CARRIERS

Field of the Invention

The present invention relates generally to the structure and manufacture of electronic printed circuit boards and chip carriers and more specifically to a particular structure of tracks in multiple layer high density electronic device carriers.

Background of the Invention

Electronic packages to be used in high speed applications have an important function beyond the classical mechanical protection for the semiconductor devices that they carry within. They ultimately need to maintain the performances offered by these semiconductor devices affecting their performances in the minimum way possible. When the switching speed of the devices goes above the 1 GHz clock rate there is the need to consider the transmission of an electrical signal as a propagation of an electromagnetic wave that is supported by a current in the circuit trace. This electromagnetic wave propagation is affected by the electronic packaging material properties such as the dielectric constant as well as the dielectric loss. There are few more, of these factors, which are related to the electronic packaging structure (construction), specifically in which way electrical circuits are placed in close or far proximity to each others. The sum of all these different factors affects the propagation of these electromagnetic waves into

the electronic package. It is known that even if a set of material and a module structural configuration are defined there may be unexpected low performance. It has been proved by simulation as well as by measurements that the propagation of the electromagnetic wave can be also severely affected by any kind of discontinuities along its propagation path. These discontinuities can be though as any change in structure, material properties, design feature that change suddenly, translates in electrical impedance (Z_0) mismatches that are known to cause reflections of the signal.

All these electronic packages need to preserve the integrity of the electromagnetic wave propagation, and this is achieved by designing and building circuit structures that have a well controlled impedance value of the transmission line. But controlling the impedance may not be enough due to the presence of other structures called parasitic (they may be capacitance, inductance and resistance) that become embedded within the package by the association of materials and electrical structures. These parasitic elements have very negligible effects in low speed digital applications but they can severely affect the signal propagation in high speed applications. They get worse with the power level value that continues to decrease (from the old TTL 5 V, down to 3.3 V, 2.5 V, 1.8 V, 1.2 V), leaving a very low margin to discriminate the "up" level from the "zero" logical status.

A good way to visualize these effects is analyzing the eye diagram of measurement of a transmitted train of signals. By the level of opening in the diagram it becomes easy to appreciate the quality of the transmitted information, as illustrated on Figures 1a and 1b. The more the

"eye" closes, as illustrated on figure 1, the more difficult is the capability to understand if the switching transition has taken place or if the shift of the signal baseline is due to background noise.

In the presented work the characterization of all the "transitions", also known as discontinuities, along the signal path have been evaluated and their contribution to the overall package performance understood. In this ranking of negative effects the plated through hole transition (PTH) has demonstrated to be one of the major contributor. The PTH transition effect has an inductive nature mated by a capacitive behavior when portion of its structures are placed close to other circuits. Such a combination acts, at high frequencies, as a low pass filter and therefore reducing the transmission line bandwidth.

In high speed applications, the design is accomplished in such a way the transmission line has a known impedance (tailored to 50 ohms), this is done by placing a reference ground plane under the layer that carries the transmission line circuit.

Impedance value is determined as follow :

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{r1}}} \ln\left(\frac{5.98H_2}{0.8W+T}\right) \qquad (1)$$

with,

$$\varepsilon_{r1} = \varepsilon_r\left[1 - \exp\left(\frac{-1.55H_1}{H_2}\right)\right] \qquad (2)$$

wherein ε_r is the epoxy laminate dielectric constant, T is the Copper thickness after plating, H_1 is the dielectric thickness plus solder mask coating thickness, H_2 is the dielectric thickness and W represents the line width as illustrated on figure 2.

This is something that can be applied to regular lines and surface circuit features. Unfortunately the traditional vertical transition does not have the possibility to offer the same referenced structure with the current standard processes in place today.

To enhance the high speed performance in the current Surface Laminar Circuit (registered trademark of International Business Corporation) and Hyper BGA (registered trademark of International Business Corporation), it is necessary to optimize the electric path for the electromagnetic wave. Design efforts have been placed to reduce and to optimize circuit discontinuities affecting the propagating wave with low pass filtering effects reducing power and distorting shapes of the propagating waves. So far, the only exception, to this optimization work has been the vertical transition, also referred as Plated Through Hole, PTH, or Resin Filled Plated Through hole, RFP, used on the SLC technology.

Figure 3a shows a partial perspective view of an electronic device carrier illustrating a standard PTH, wherein conductive layers 300 and 305 are separated by the core 310 of the electronic device carrier that may comprise or not conductive layers. Core 310 is made of dielectric material such as epoxy. Conductive layer 300 comprises a track 315 for transmitting high speed signal that is

shielded by conductive track 320. Likewise, conductive layer 305 comprises track 325 that is shielded by conductive track 330. Conductive tracks 315 and 325 are connected thanks to PTH 335. PTH 335 is done by drilling core 310 and filling the hole with conductive material or plating the hole vertical wall.

Figure 3b depicts a partial cross section view of an electronic device carrier illustrating standard PTH and RFP. For sake of illustration, the core 350 of the electronic device carrier comprises two internal conductive layers and a conductive layer on each side, i.e. core 350 has 2 signal layers and 2 power planes also known in the industry as a 2S2P core. Each side of the core is covered with an dielectric material 355, e.g. epoxy, on which external conductive tracks may be designed, e.g. conductive track 360. Electrical connections between tracks belonging to core 350 are done either through PTH or RFP as mentioned above. In this example, RFP 365 connects several conductive tracks of core 350. RFP are done by drilling core 350, plating the hole with conductive material to form a cylinder and filling this cylinder with dielectric material such as epoxy, as illustrated. Likewise, PTH 370 connects several conductive tracks of core 350.

These vertical transitions affects 100% of high speed signals that need to go through the central core of laminate electronic device carriers. Therefore these transitions are now becoming the highest impact on signal transmission.

Summary of the Invention

Thus, it is a broad object of the invention to remedy the shortcomings of the prior art as described here above.

It is another object of the invention to provide a track structure adapted for carrying high speed signals.

It is a further object of the invention to provide a track structure adapted for carrying high intensity currents.

The accomplishment of these and other related objects is achieved by a coaxial via structure in an electronic device carrier adapted to connect a first conductive track of a first conductive layer to a second conductive track of a second conductive layer and a third conductive track of said first conductive layer to a fourth conductive track of said second conductive layer, a dielectric layer being disposed between said first and second conductive layers, said coaxial via structure comprising :

- a first conductive via connecting said first and second conductive tracks ;
- a second conductive via, surrounding said first conductive via, connecting said third and fourth conductive tracks ; and,
- a dielectric material disposed between said first and second conductive vias ;

said first and second conductive vias having a common axis, approximately perpendicular to said conductive layers.

Further advantages of the present invention will become apparent to the ones skilled in the art upon examination of the drawings and detailed description. It is intended that any additional advantages be incorporated herein.

Brief Description of the Drawings

Figure 1 comprising figures 1a and 1b, is an example of eye-diagrams illustrating the transmission of a signal. Figure 1a represents a close eye wherein a switching transition is not easy to distinguish from background noise and figure 1b represents an open eye illustrating a switching transition.

Figure 2 depicts a cross-section view of an electronic device carrier to illustrate the way of determining the controlled impedance signal to reference plane relation.

Figure 3 , comprising figures 3a and 3b, shows a partial perspective and a plan view of an electronic device carrier illustrating standard plated through hole and resin filed plated through hole.

Figure 4 illustrates a cross-section view of an electronic device carrier comprising the coaxial via structure of the invention.

Figures 5 represents a plan view of a conductive layer of an electronic device carrier to illustrate the way of determining the impedance in a coaxial structure.

Figure 6 , comprising figures 6a and 6b, illustrates the use of shielding vias in conjunction with the coaxial via structure of the invention.

Figures 7 and 8 represent implementation examples of the coaxial via structure of the invention for an electronic device carrier comprising several conductive layers above and under the core when the manufacturing process does not allow to create a coaxial via structure across the full electronic device carrier.

Figure 9 illustrate how vias have to be preferably disposed to carry high speed signal when three of them are used to connect conductive tracks of two adjacent conductive layers.

Figures 10 and 11 illustrate examples of the shape of the conductive layer track on which vias are connected that may replace the annular rings used in the implementation example of figures 7 and 8.

Figures 12 and 13 represent diagrams illustrating the advantages provided by the coaxial via structure of the invention in terms of electrical behavior by comparing the output of a design example for a known electronic device (curves a) with an electronic device including the coaxial via structure of the invention (curves b).

Detailed Description of the Preferred Embodiment

According to the invention there is provided a coaxial via structure that may be implemented in an electronic device carrier comprising several conductive layers. Such coaxial via structure can deliver a referenced shielding element to the high speed line between conductive layers such as it becomes now possible to be in compliance with geometry requirements to achieve a controlled impedance along this transition. The laminate electronic device carrier comprising the coaxial via structure according to

the invention is processed through standard manufacturing operations.

Figure 4 illustrates a partial cross section view of an electronic device carrier illustrating the coaxial via structure of the invention. In this example, the electronic device carrier is based on a 2S2P core 400 that comprises two internal conductive layers and a conductive layer on each side that are covered with an dielectric material, e.g. epoxy, on which external conductive tracks may be designed, like the one described by reference to figure 3b. The coaxial via structure 405 consists in a resin filled plated through hole wherein a second hole is done and filled with conductive material so as to create two coaxial conductive tracks 410 and 415. Conductive track 415 is used to carry high speed signal while conductive track 410 is used to shield this high speed signal and is preferably connected to ground.

The coaxial via structure 405 provides a referenced shielding element to the high speed line such that it is possible to be in compliance with geometry requirements to achieve a controlled impedance value. For example, the impedance is computed according to the following equation for copper conductive tracks :

$$Z_c = \frac{60}{\sqrt{\varepsilon_r}} \cdot \ln\left(\frac{R_2}{R_1}\right) \qquad (3)$$

wherein R_1 is the radius of the central coaxial track 415, R_2 is the radius of the external coaxial track 410 and ε_r is the dielectric constant of the dielectric material that separates both tracks, as illustrated on figure 5 that

represents a partial plan view of the electronic device carrier along plan A-A of figure 4.

The coaxial via structure is accomplished through a sequence of operations already used in the standard manufacturing processes. For example, the coaxial via structure may be done by drilling with mechanical drill bit the larger diameter, plating the drilled hole, filling the plated hole with a dielectric material, e.g. epoxy resins, polyphenylene ther (PPE), annylated polyphenylene ether (APPE), benzocyclobutene (BCB), cyanate (triazine) resins, polytetrafluorethylene (PTFE), bismaleimide triazine (BT) resins, polyimide, polyester, phenolic or poly(phenyleneetherketone) (PEEK), drilling by the same or another method such as laser using excimer laser, CO2 laser or Nd-YAG (neodimium - yttrium aluminum garnet) infrared laser a new pass through hole in the center of the larger plated hole filled with dielectric material, and finally plating the latter hole, for example with electroless copper process.

In a preferred embodiment, the electronic device carrier comprises coplanar wave-guide micro-strip structures for the top and bottom layers. Considering figure 6a illustrating a partial plan view of an electronic device carrier, there is shown a track, referred to as 600, ending with pad 605, which may be connected to the central track of the coaxial via structure of the invention, which is used for transmitting a high speed signal. A coplanar track, referred to as 610, is arranged around signal track 600 and may be formed in the same conductive layer and connected to the ground, as illustrated. Furthermore, several shielding vias, generically referred to as 615, are arranged on the coplanar wave-guide shielding track to be connected to a coplanar wave-guide shielding track of an adjacent layer.

Figure 6b shows a perspective view of the particular configuration presented on figure 6a that comprises only one shielding via 615 for sake of clarity. Conductive layer 620 comprises tracks 600 and 610. Conductive layer 625 that is an external surface layer of core 630 comprises track 635 that is partially superimposed to track 610. Conductive layers 620 and 625 are separated by dielectric layer 640. Electrical connection between tracks 610 and 635 is done through several via 615 (only one being represented for sake of clarity). Thus, vias 615 shield the central coaxial track 645, connected to track 600 that carry high speed signals, between conductive layers 620 and 625. Track 635 is connected to the external coaxial track 650 that shield the central coaxial track 645 inside the core 630. As mentioned above, tracks 610, 635 and 650 and vias 615 are preferably connected to ground.

Depending upon the process used to create the coaxial via structure in the electronic device carrier, it could be possible or not to make the central and/or external track of the coaxial via structure in the layers that are located above and under the core. It is possible to create central and external track of the coaxial via structure, the result looks like the combination shown on figure 4 wherein more conductive layers may be used. In such case, the structure preferably comprises the shielding vias presented on figure 6.

Figure 7 presents another preferred embodiment of the coaxial via structure to be used when the electronic device carrier comprises more than two conductive layers on one side of the core and the manufacturing process does not allow to create the external track of the coaxial via structure in the layers that are located above and under the

core. In such case, the electrical connection between two shielding tracks belonging to two adjacent conductive layers is done through several vias. The track portion to which vias are connected is designed so that it provides an efficient shielding effect. The shape of these tracks can be any geometrical solid metal shape. In a preferred embodiment, the shape of this track portion looks like an annular ring. Vias arranged between a second and a third conductive layers are not disposed at the same locations than vias arranged between a first and the second conductive layers, when considering z axis, to avoid manufacturing and electrical connection drawbacks.

With reference in particular to figure 7, there is depicted a staked via structure combined with a coaxial via structure, adapted to connect conductive tracks belonging to two different conductive layers that are separated by a third conductive layer. In this example, a first conductive layer 700a is located on the surface of the core 705, a second conductive layer 700b is located above conductive layer 700a, conductive layers 700a and 700b being separated by a dielectric layer 710a, and third conductive layer 700c is located above conductive layer 700b, conductive layers 700b and 700c being separated by a dielectric layer 710b. The depicted structure comprises a central track 715 of the coaxial via structure that comes from core 705, goes across conductive layers 700a and 700b and is connected to conductive track 720 of conductive layer 700c. The first conductive layer 700a comprises one conductive track having the shape of an annular ring, referred to as 725 that is connected to the external track 730 of the coaxial via structure. Four vias 735-1 to 735-4 (generically referred to as 735) are connected to the annular ring 725 so as to provide an electrical connection with conductive track 740

having also the shape of an annular ring, belonging to conductive layer 700b, adjacent to conductive layer 700a. As mentioned above, conductive layers 700a and 700b are separated by a dielectric layer 710a. Vias 735-1 to 735-4 are symmetrically arranged on conductive tracks 725 and 740 so as to provide an efficient shielding effect. Naturally, to improve shielding effect, more vias 735 may be used. Similar structure is duplicated between conductive layers 700b and 700c, taking into account signal track 720. Three vias 750-1 to 750-3 (generically referred to as 750) are connected to the annular ring 740 so as to provide an electrical connection with conductive track 755, belonging to conductive layer 700c. Each vias 750 is preferably connected to conductive track 740 such that the distances between this via and the two closest vias 735 are the same to obtain a uniform shielding effect. In the illustrated example of figure 7, conductive tracks 725, 740 and a portion of conductive track 755 are of the same size and aligned along z axis, vias 735 are set at positions 0°, 90°, 180° and 270° considering the center of conductive tracks 725 and 740 with z axis and vias 750 are set at positions 45°, 135° and 225°.

Figure 8 presents another preferred embodiment of the coaxial via structure to be used when the electronic device carrier comprises more than two conductive layers on one side of the core and the process does not allow to drill the full electronic device carrier thickness, i.e. to create the conductive tracks of the coaxial via structure in the layers that are located above and under the core. This situation arises in particular when larger diameter hole is done with a mechanical drill bit that may damage the conductive tracks designed in the external layers. In such case, the electrical connection between two tracks belonging to two adjacent

conductive layers is done through several vias, at least two and preferably four for connecting tracks carrying high speed signals. The track portion to which vias are connected is designed so that it provides a symmetrical distribution of signal current across these vias and an efficient shielding effect. The shape of these tracks can be any geometrical solid metal shape. In a preferred embodiment, the shape of this track portion looks like an annular ring. Vias arranged between a second and a third conductive layers are not disposed at the same locations than vias arranged between a first and the second conductive layers, when considering z axis, to avoid manufacturing and electrical connection drawbacks. As illustrated, the same structure is done for the central and external tracks of the coaxial via structure.

Thus, there is depicted on figure 8 a staked via structure combined with a coaxial via structure, adapted to connect conductive tracks belonging to two different conductive layers that are separated by a third conductive layer. In this example, like the one described by reference to figure 7, a first conductive layer 800a is located on the surface of the core 805, a second conductive layer 800b is located above conductive layer 800a, conductive layers 800a and 800b being separated by a dielectric layer 810a, and third conductive layer 800c is located above conductive layer 800b, conductive layers 800b and 800c being separated by a dielectric layer 810b. The core 805 comprises a coaxial via structure having a central conductive track 815 and an external conductive track 820. Two concentric conductive tracks 825a and 830a are designed in conductive layer 800a such that the are aligned with conductive tracks 815 and 820, conductive track 825a being connected to conductive track 815 and conductive track 830a being connected to

conductive track 820. Conductive tracks 825a and 830a have the shape of annular rings. Likewise, conductive layer 800b comprises two concentric conductive tracks 825b and 830b having also the shape of annular rings and being aligned with conductive tracks 825a and 830a according to z axis. Two sets of vias connect conductive tracks 825a and 830a to conductive tracks 825b and 830b, respectively. Four vias 835-1 to 835-4 (generically referred to as 835) of the first set of vias are connected to conductive track 825a so as to provide an electrical connection with conductive track 825b. Vias 835-1 to 835-4 are symmetrically arranged on conductive tracks 825a and 825b so that the electrical signal current flow is uniformly distributed among them. Likewise, four vias 840-1 to 840-4 (generically referred to as 840) of the second set of vias are connected to conductive track 830a so as to provide an electrical connection with conductive track 830b. Vias 840-1 to 840-4 are symmetrically arranged on conductive tracks 830a and 830b so as to provide an efficient shielding effect that may naturally be improved by increasing the number of vias 840. Similar structure is duplicated between conductive layers 800b and 800c, taking into account high speed signal track 845 and shielding track 850 of conductive layer 800c. Two sets of vias connect conductive tracks 825b and 830b to conductive tracks 845 and 850, respectively. Four vias 855-1 to 855-4 (generically referred to as 855) of the first set of vias are connected to conductive track 825b so as to provide an electrical connection with conductive track 845. Vias 855-1 to 855-4 are symmetrically arranged on conductive tracks 825b and 845 so that the electrical signal current flow is uniformly distributed among them. Each vias 855 is preferably connected to conductive track 825b such that the distances between this via and the two closest vias 835 are the same to obtain a uniform distribution of electrical signal

current flow from vias 835 to vias 855. In the illustrated example of figure 8, conductive tracks 825a, 825b and a portion of conductive track 845 are of the same size and aligned along z axis, vias 835 are set at positions 0°, 90°, 180° and 270° considering the center of conductive tracks 825a and 825b with z axis and vias 855 are set at positions 45°, 135°, 225° and 315°. Likewise, three vias 860-1 to 860-3 (generically referred to as 860) of the second set of vias are connected to conductive track 830b so as to provide an electrical connection with conductive track 850. Vias 860-1 to 860-3 are symmetrically arranged on conductive tracks 830a and 830b so as to provide an efficient shielding effect that may naturally be improved by increasing the number of vias 860. Each vias 860 is preferably connected to conductive track 830b such that the distances between this via and the two closest vias 840 are the same to obtain a uniform shielding effect. In this example, conductive tracks 830a, 830b and a portion of conductive track 850 are of the same size and aligned along z axis, vias 840 are set at positions 0°, 90°, 180° and 270° considering the center of conductive tracks 830a and 830b with z axis and vias 860 are set at positions 45°, 135° and 225°.

It is to be noticed that a similar structure may be done without conductive track 825a if the diameter of central track 815 is large enough to connect vias 835-1 to 835-4.

Now turning to figure 9, there is shown how vias have to be preferably disposed when three of them are used to connect conductive tracks of two adjacent conductive layers, particularly when connecting tracks carrying high speed signals. As mentioned above, the vias are preferably disposed so as to distribute uniformly the electrical signal

current flow among the vias. Figure 9 comprises two annular rings 900-1 and 900-2 that are formed in two adjacent conductive layers, annular ring 900-1 being formed in the upper conductive layer. Thus, considering annular rings 900-1 and 900-2, the three vias 905-1, 905-2 and 905-3 that link these annular rings must be placed on lines forming an angle of $\alpha = 360°/n = 120°$ according to z axis, n being the number of vias used to connect two adjacent conductive layer in the stacked via structure, i.e. $n = 3$ in this example. Furthermore, the distances d between the vias and the center of the annular rings 900-1 and 900-2 must be the same. Likewise, the three vias 910-1, 910-2 and 910-3 that connect annular ring 900-1 to a conductive track of an upper conductive layer and the three vias 915-1, 915-2 and 915-3 that connect annular ring 900-2 to a conductive track of a lower conductive layer have to be disposed according to the position of vias 905-1, 905-2 and 805-3. Vias 910-1, 910-2 and 910-3 must be placed on lines forming an angle of $\alpha = 120°$, perpendicular to z axis, these lines forming an angle of $\alpha/2 = 60°$ with the lines on which vias 905-1, 905-2 and 905-3 are disposed. The distance d' between the vias and the center of the annular rings 900-1 and 900-2 must be the same but does not need to be the same as the distance d between vias 905-1, 905-2 and 905-3 and the center of the annular rings 900-1 and 900-2.

Figures 10 and 11 show examples of conductive tracks that may replace the above mentioned annular rings of the stacked via structure. Each figure comprises the conductive tracks of two adjacent conductive layers and an example of the position of the vias when four of them are used to connect to adjacent conductive tracks. These conductive tracks show a relative rotation of 45° on each of the given

layers 900-n (n being the number of the layers available on the different side of the core laminate structures). This configuration with inserted slots in the annular ring or a design with lobes avoid to establish loops for currents that will generate adverse condition to the propagation of the electromagnetic wave.

With reference in particular to figure 12, there is depicted a diagram representing the phase versus the frequency for a known electronic module wherein electrical connection between conductive layers are not shielded (curve a) and for an electronic device comprising the coaxial via structure of the invention (curve b). This diagram shows that even if mechanically these two structures are comparable allowing the vertical (Z) path transition of the conductive tracks, they shows a complete different electrical behaviour. This difference translates in different delays in the transmission of an incident electrical signal. In an application example using signal running at 15 GHz (equal to a cycle time of about 66 ps) the two structures show a difference delay of about 17 ps on the incident wave, as illustrated on figure 13 wherein curve s corresponds to the input signal. Such a delay difference represents a quarter of the total cycle time allowing, in the case of stacked structure usage, a better signal management with a lower distortion effect on signal fronts.

Naturally, in order to satisfy local and specific requirements, a person skilled in the art may apply to the solution described above many modifications and alterations all of which, however, are included within the scope of protection of the invention as defined by the following claims.

Claims:

1. A coaxial via structure (405) in an electronic device carrier adapted to connect a first conductive track of a first conductive layer to a second conductive track of a second conductive layer and a third conductive track of said first conductive layer to a fourth conductive track of said second conductive layer, a dielectric layer being disposed between said first and second conductive layers, said coaxial via structure comprising :

- a first conductive via (415) connecting said first and second conductive tracks ;

- a second conductive via (410), surrounding said first conductive via (415), connecting said third and fourth conductive tracks ; and,

- a dielectric material disposed between said first and second conductive vias (415, 410) ;

said first and second conductive vias (415, 410) having a common axis, approximately perpendicular to said conductive layers.

2. The coaxial via structure of claim 1 wherein the core (400) of said electronic device carrier is disposed between said first and second conductive layers.

3. The coaxial via structure of either claim 1 or claim 2 further comprising a third conductive layer wherein said third conductive track is designed.

4. The coaxial via structure of claim 3 further comprising a fourth conductive layer wherein said fourth conductive track is designed.

5. The coaxial via structure of either claim 3 or 4 further comprising a fifth conductive track (610) designed in said first conductive layer, surrounding partially said first conductive track (600) and being aligned with at least one part of said third conductive track (635) according to the axis perpendicular to said conductive layers, and at least one conductive via (615) connecting said fifth and third conductive tracks (610, 635).

6. The coaxial via structure of either claim 3 or 4 further comprising at least one additional conductive layer (700b) arranged between said first and third conductive layers (700c, 700a), dielectric layers (710b, 710a) being disposed between said first conductive layer (700c), said at least one additional conductive layer (700b) and said third conductive layer (700a), wherein said at least one additional conductive layer (700b) comprises a conductive track (740) being aligned with at least one part of said third conductive track (725) according to the axis perpendicular to said conductive layers and connected to said third conductive track (725) with at least one conductive via (735).

7. The coaxial via structure of claim 6 further comprising an additional conductive track (755) designed in said first conductive layer (700c), surrounding partially said first conductive track (720) and being aligned with at least one part of said conductive track (740) of said at least one additional conductive layer (700b) according to the axis

perpendicular to said conductive layers, and at least one conductive via (750) connecting said additional conductive track (755) and said conductive track (740) of said at least one additional conductive layer (700b).

8. The coaxial via structure of anyone of claims 1 to 7 further comprising a supplementary conductive layer (800b) such that said first conductive layer (800a) is located between said second conductive layer and said supplementary conductive layer (800b), a dielectric layer (810b) being disposed between said first conductive layer (800a) and said supplementary conductive layer (800b), wherein said supplementary conductive layer (800b) comprises a first supplementary conductive track (825b) being aligned with at least one part of said first conductive track (825a) according to the axis perpendicular to said conductive layers and connected to said first conductive track (825a) with at least two conductive via (835).

9. The coaxial via structure of claim 8 wherein said supplementary conductive layer (800b) further comprise a second supplementary conductive track (830b), surrounding, at least partially, said first supplementary conductive track (825b), being aligned with at least one part of said third conductive track (830a) according to the axis perpendicular to said conductive layers and connected to said third conductive track (830a) with at least one conductive via (840).

10. A method for building a coaxial via structure as described in either claim 1 or claim 2, said method comprising the steps of :

- drilling a first hole in the electronic device carrier ;
- plating said first hole ;
- filling said plated hole with a dielectric material ;
- drilling a second hole in said filled plated hole such that said first and second hole share a common axis and the diameter of said second hole is less than the one of said first hole ; and,
- plating said second hole.

COAXIAL VIA STRUCTURE FOR OPTIMIZING SIGNAL TRANSMISSION IN MULTIPLE LAYER ELECTRONIC DEVICE CARRIERS

Abstract

A coaxial via structure (405) adapted to transmit high speed signals or high intensity current through conductive layers of an electronic device carrier is disclosed. The coaxial via structure comprises a central conductive track (415) and an external conductive track (410) separated by a dielectric material and is created in the core of the electronic device carrier or the full thickness of the electronic device depending upon the request and the manufacturing process. For example, creating the coaxial via structure may consist in drilling with mechanical drill bit the larger diameter, plating the drilled hole, filling the plated hole with a dielectric material, drilling by the same or another method such as laser a new pass through hole in the center of the larger plated hole filled with dielectric material, and finally plating the latter hole. In a further embodiment, the coaxial via structure is combined with a stacked via structure so as to carry efficiently high speed signals across the electronic device carrier even if the manufacturing process does not allow to create a full coaxial via structure across the electronic device carrier.

Figure 4.

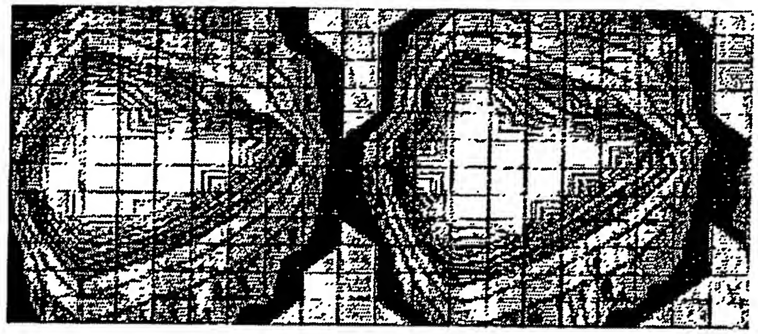


Figure 1a

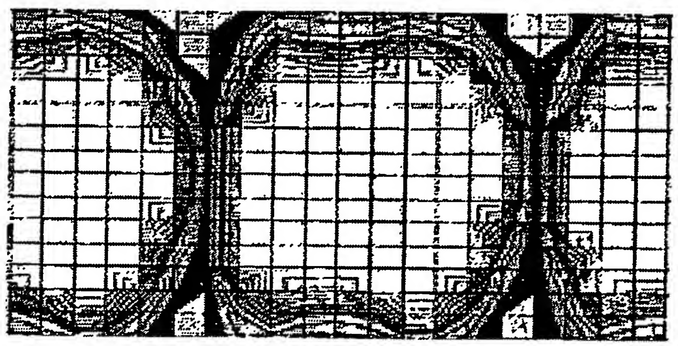


Figure 1b

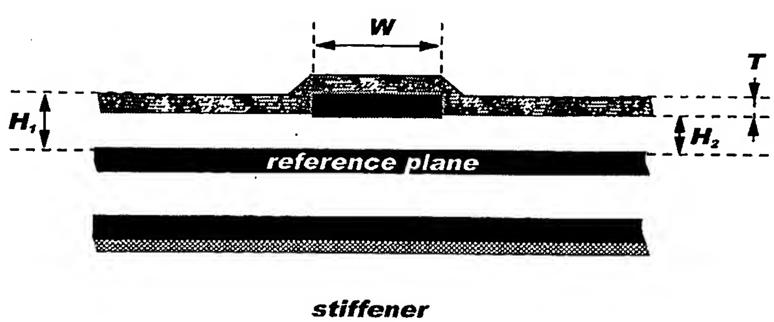


Figure 2

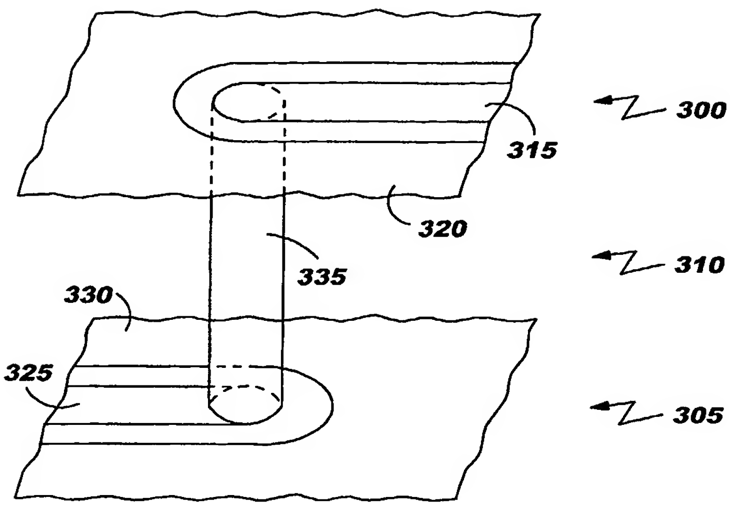


Figure 3a
(prior art)

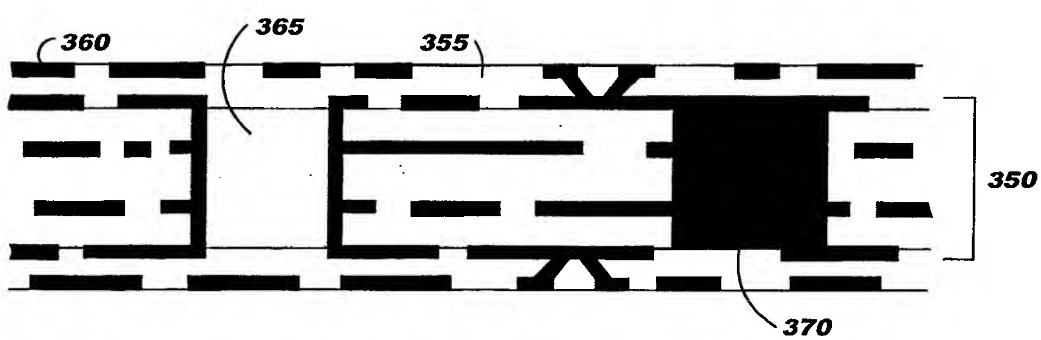


Figure 3b
(prior art)

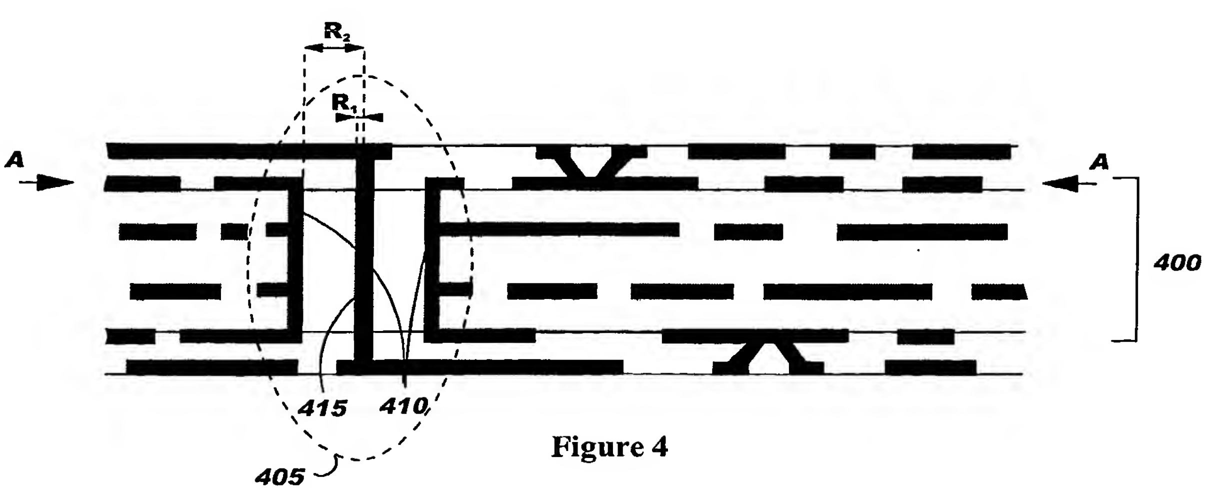


Figure 4

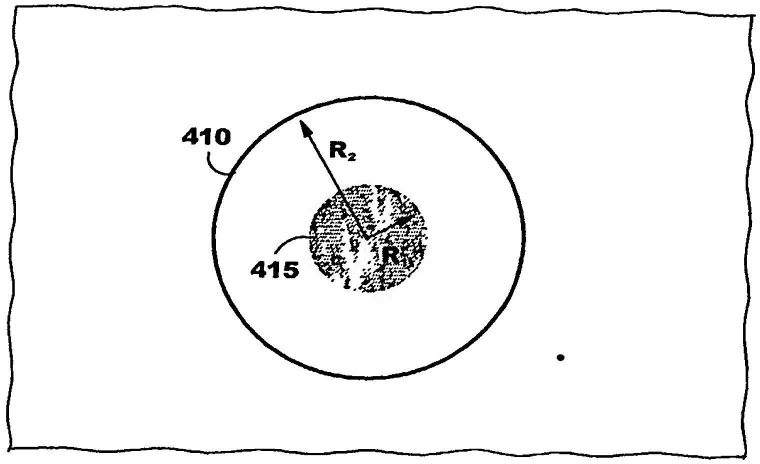


Figure 5

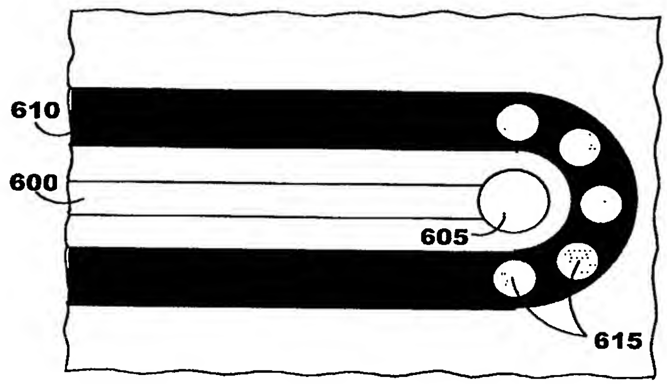
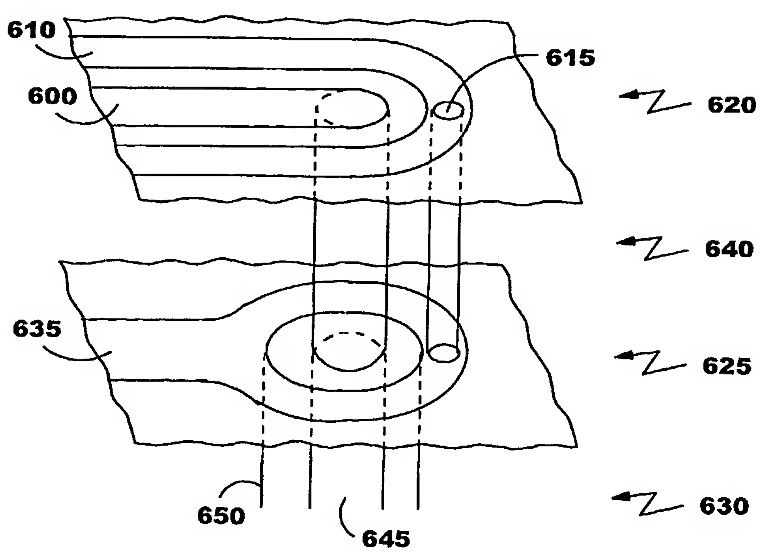
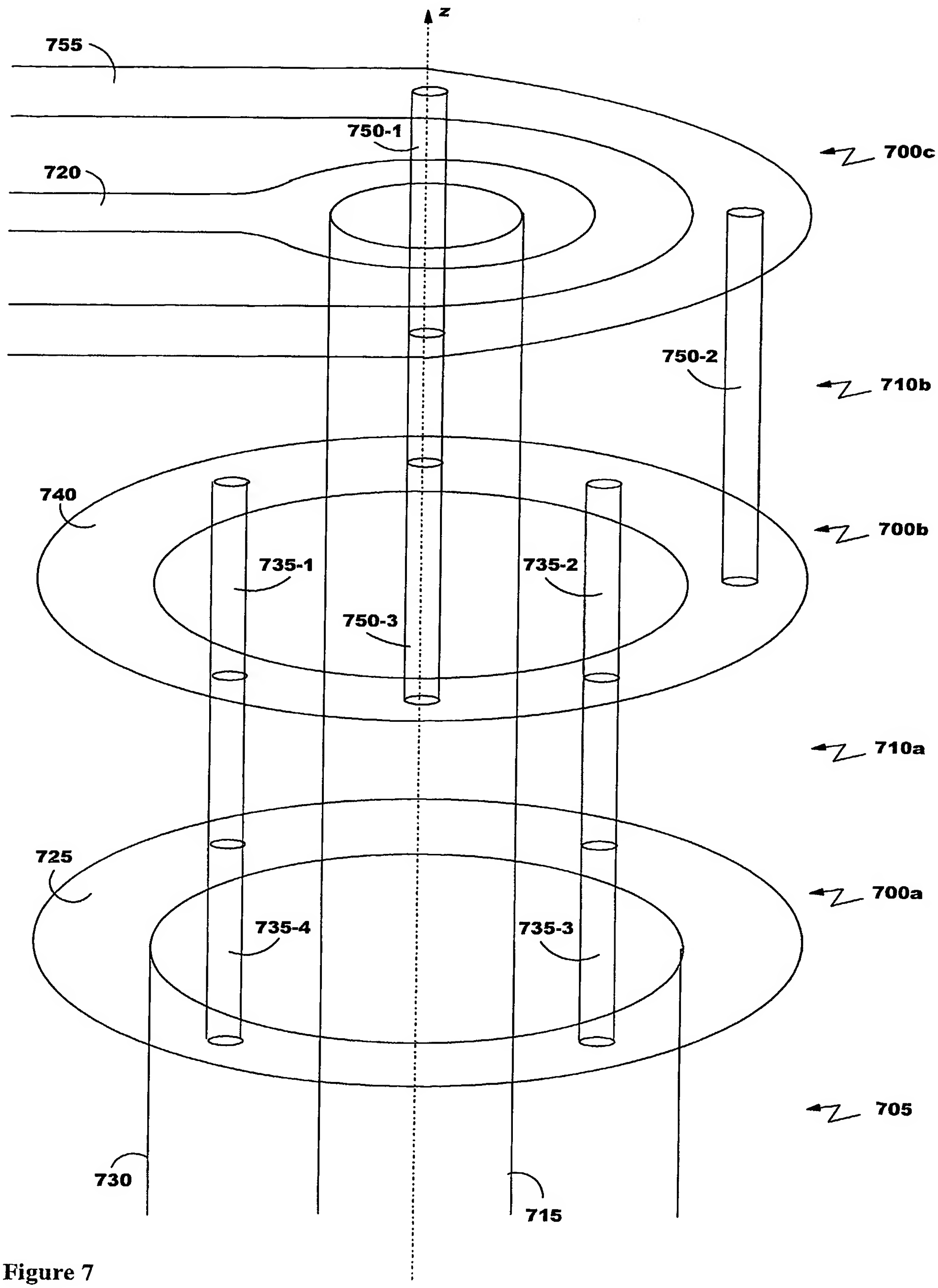


Figure 6a

Figure 6b

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720
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710b
740
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735-1
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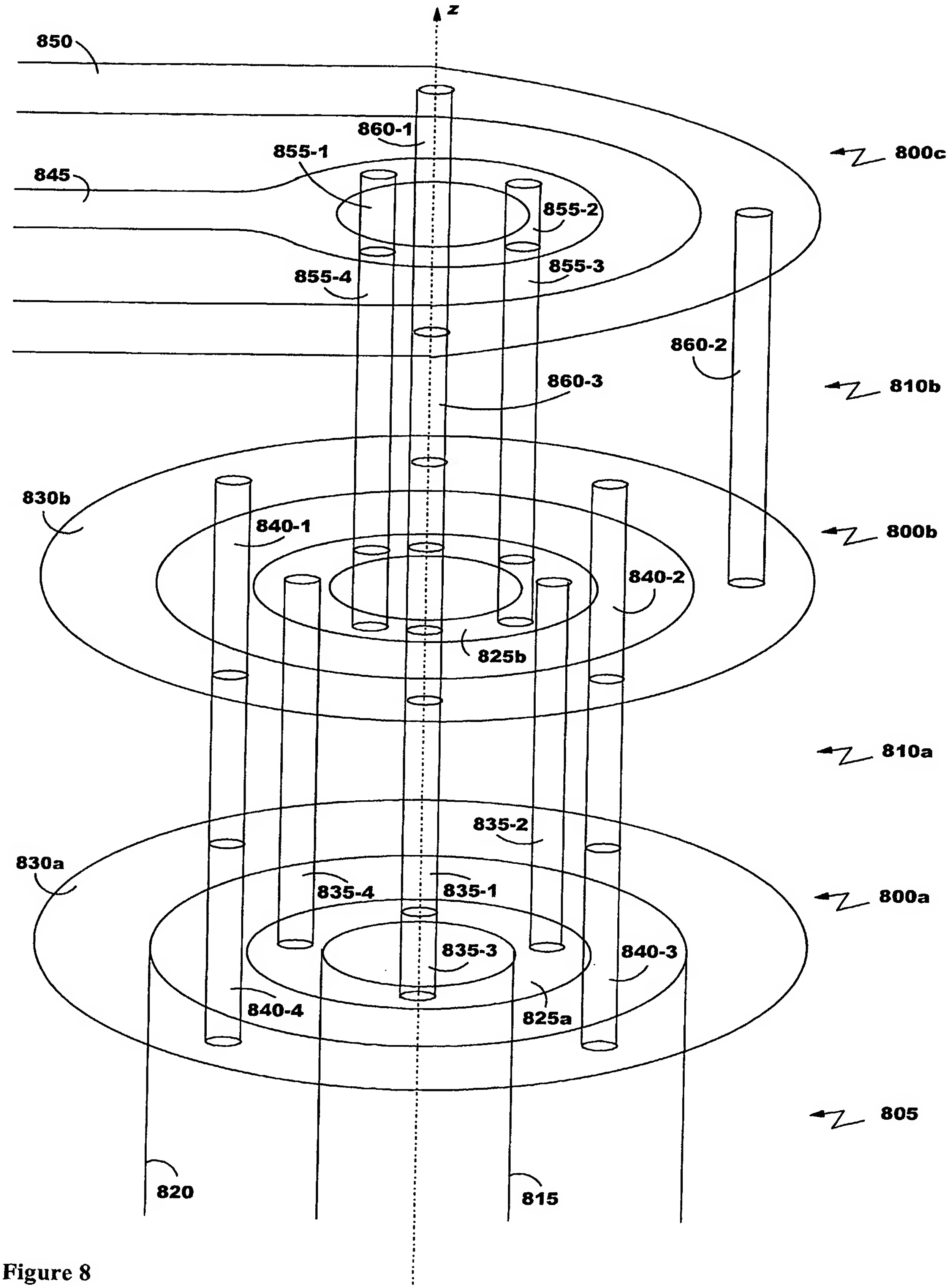
735-4
735-3
705
730
715

Figure 7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820
815

Figure 8

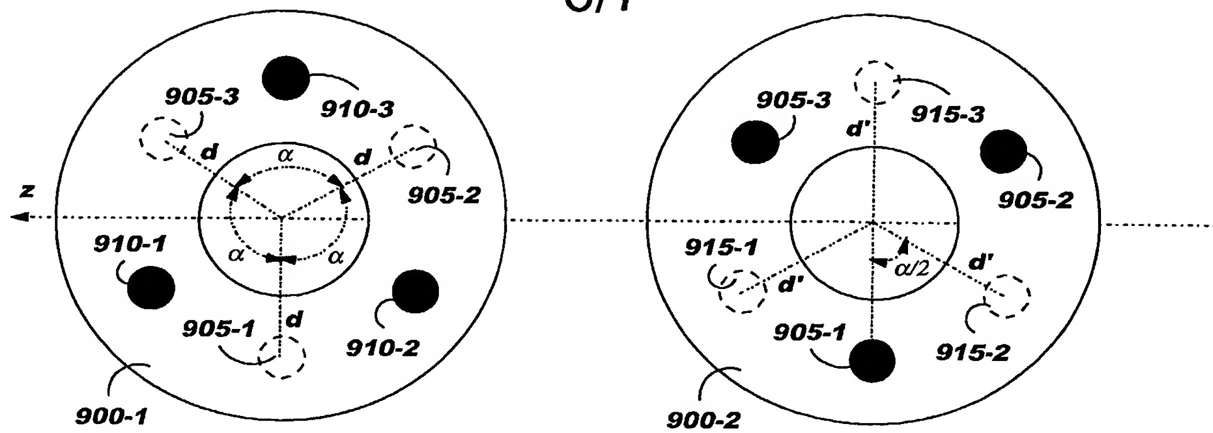

Figure 9

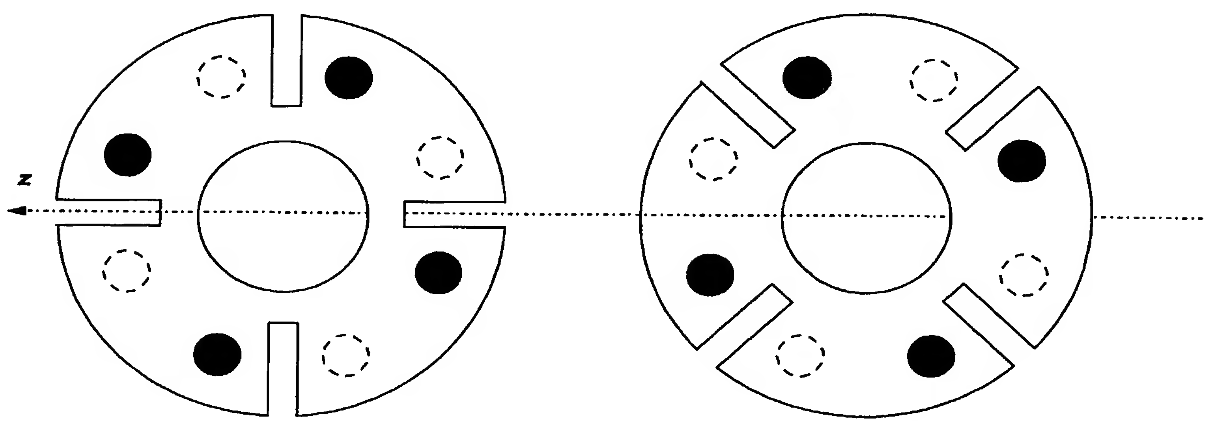

Figure 10

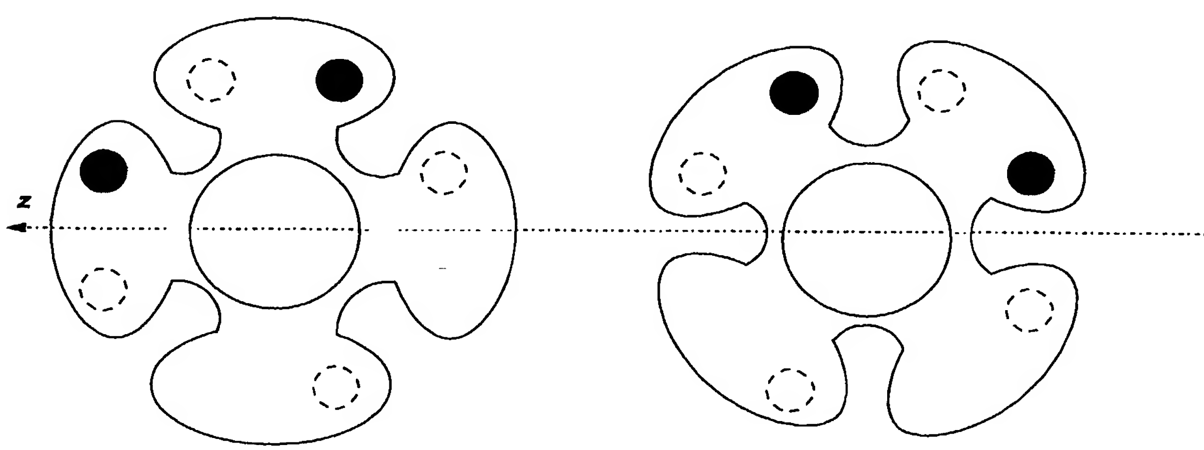

Figure 11

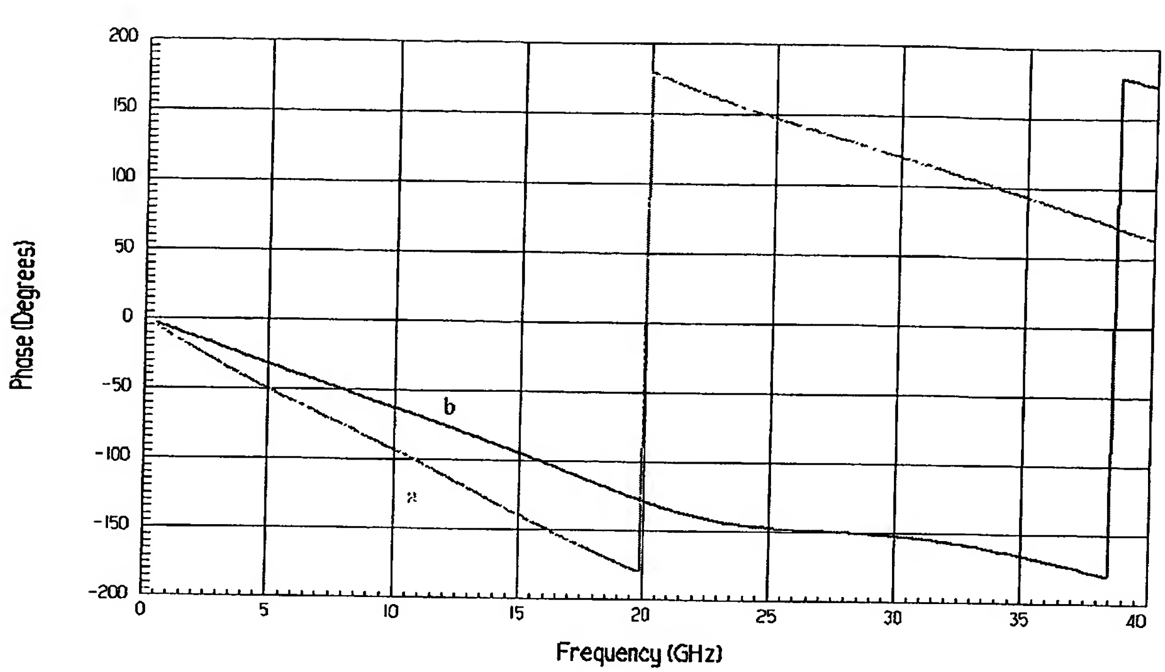

Figure 12

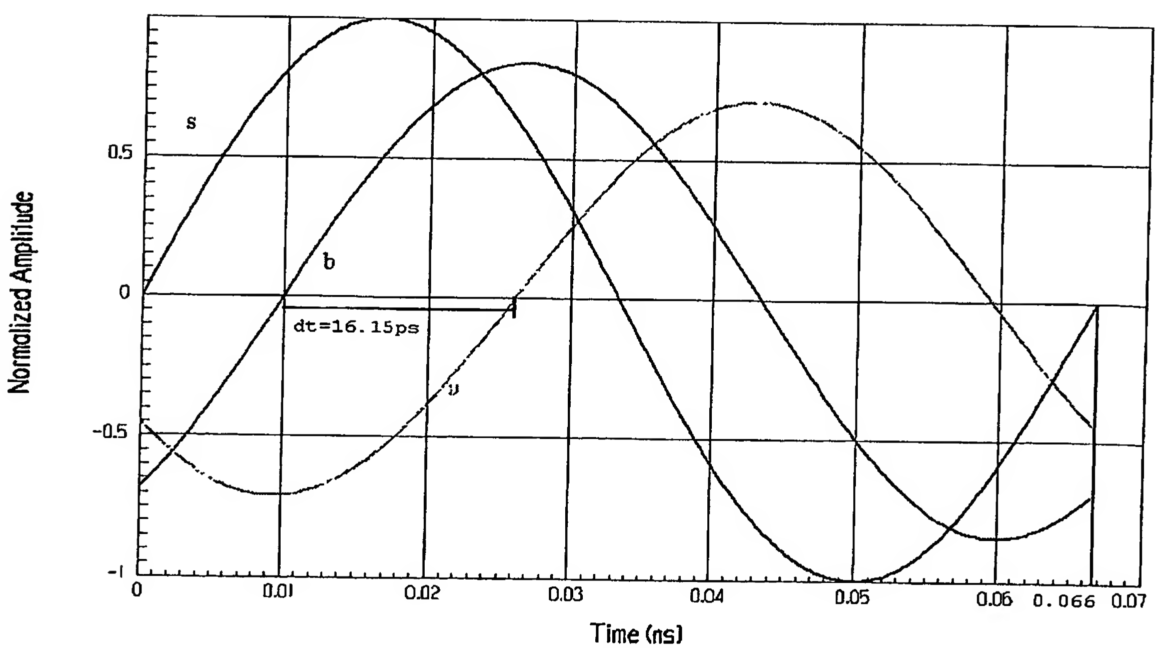

Figure 13